



UNIVERSITY OF CAGLIARI

DIEE - Department of Electrical and Electronic Engineering

Spiking Neural Networks for near-sensor processing: an open-hardware experience.

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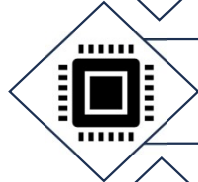
Topics Covered



Introduction



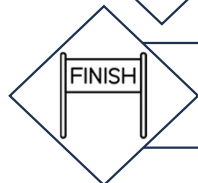
Spiking Neural Networks



Open-source EDA tools: OpenLane

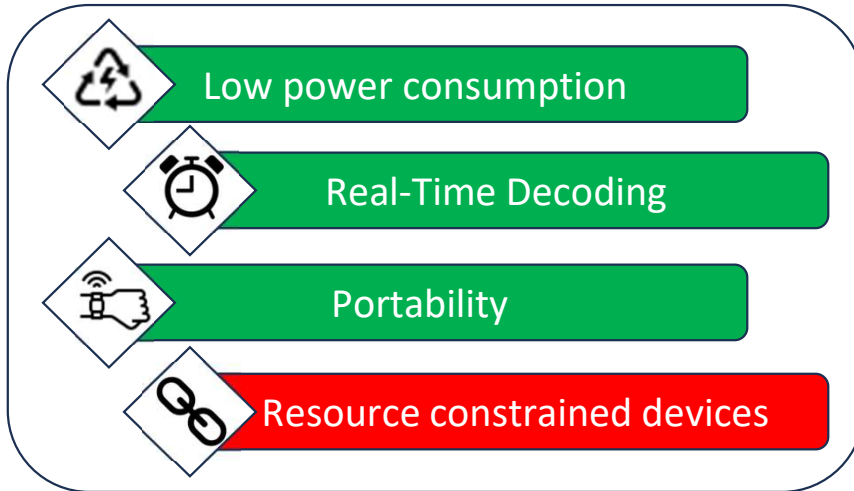


Results

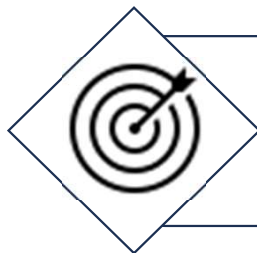
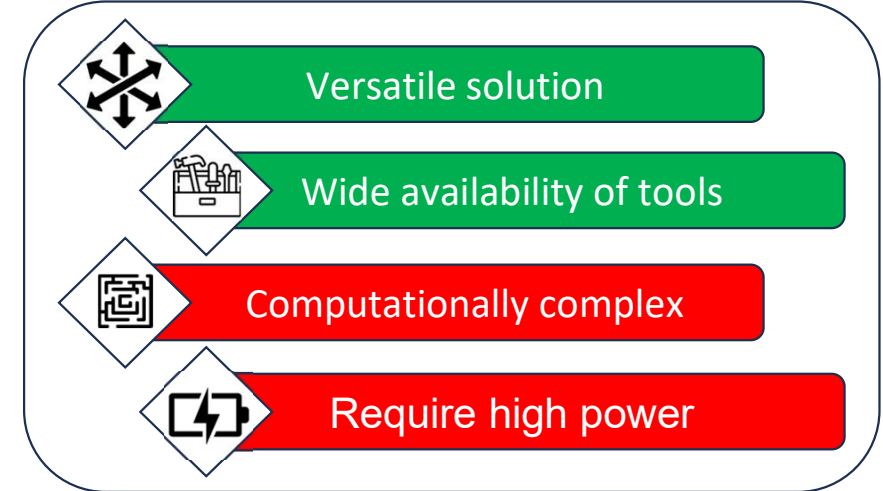


Conclusion and Future Works

Edge Computing

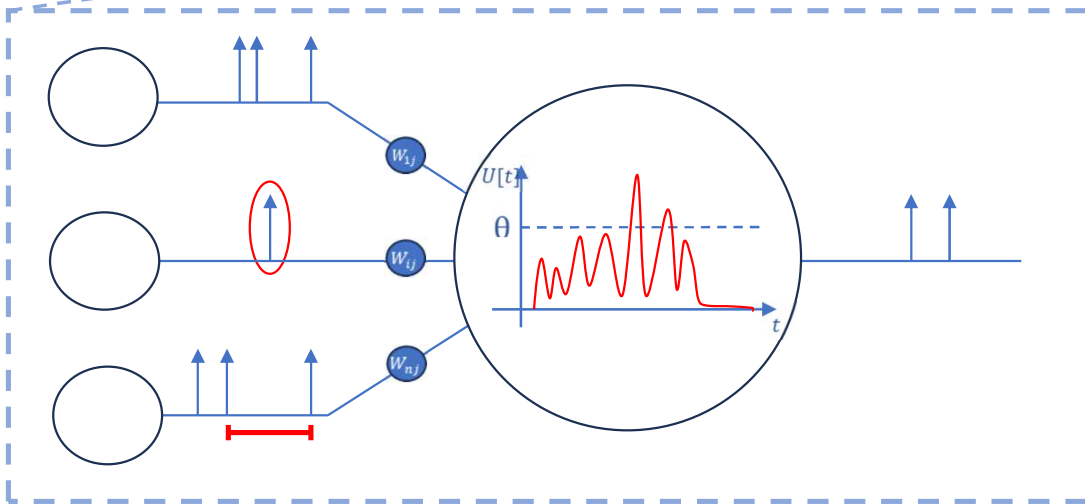
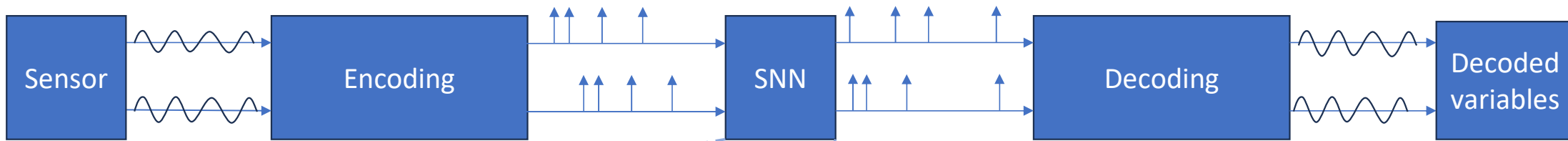


Artificial Intelligence



The main goal of my research is to develop optimized systems based on the **edge computing paradigm** for executing **artificial intelligence** algorithms.

Spiking Neural Networks (SNNs)



ADVANTAGES

- Event-based processing
- Low computation complexity
- High biocompatibility

DISADVANTAGES

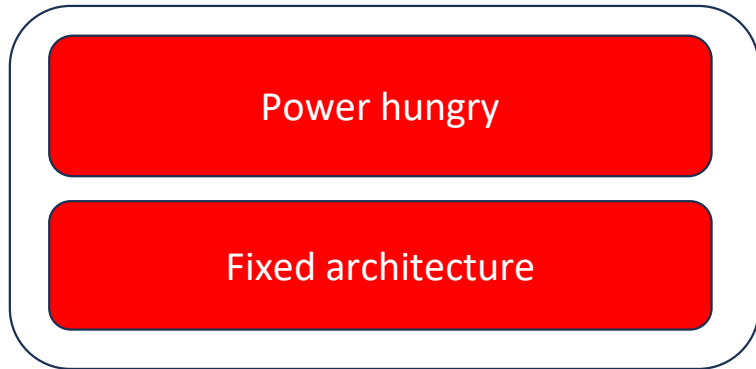
- We need to encode into spike-trains the analog input
- We need to decode into analog value the output spike-trains



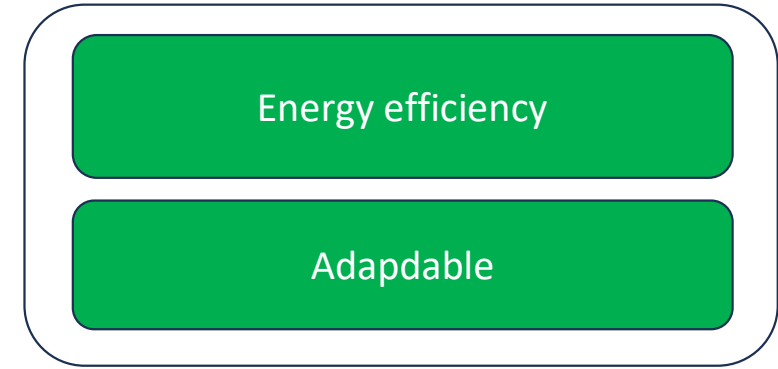
Spiking Neural Networks (SNNs)



State of the art SNN accelerator

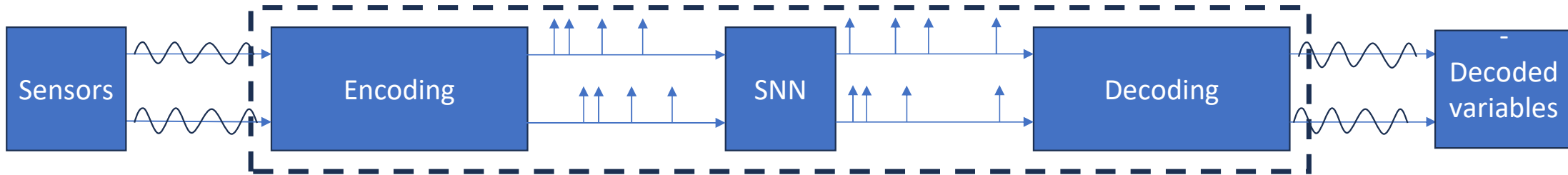


We want

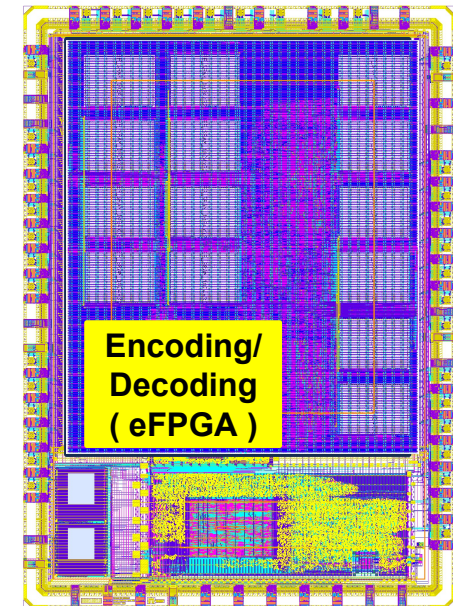
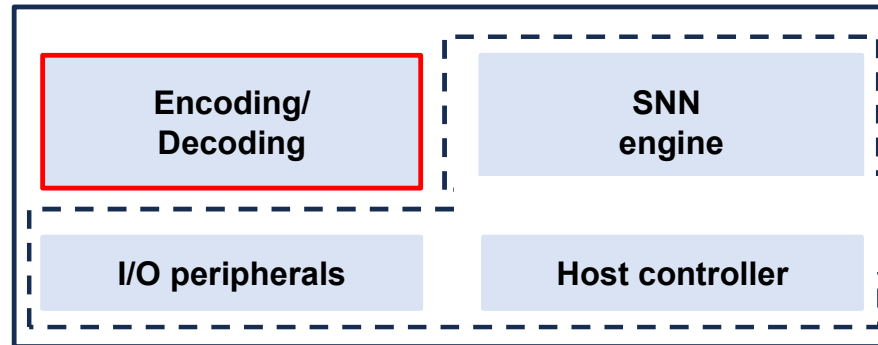


[1] Antonio Vitale et al. "Neuromorphic Edge Computing for Biomedical Applications: Gesture Classification Using EMG Signals". In: IEEE Sensors Journal 22.20 (2022), pp. 19490–19499. doi: 10.1109/JSEN.2022.3194678.
[2] "Classification and regression of spatio-temporal signals using NeuCube and its realization on SpiNNaker neuromorphic hardware". In: Journal of Neural Engineering 16.2 (2019), p. 026014. doi: 10.1088/1741-2552/aafabc

Spiking Neural Network (SNNs)



Reconfigurable ASIC





Open-source EDA Tools



Significantly reduce entry barriers for students and researchers in chip design.

Allow researchers and designers to collaborate easily.

Interesting for innovations, research, and development.

Different tools that provide a complete flow from RTL to GDSII are already available, such as:

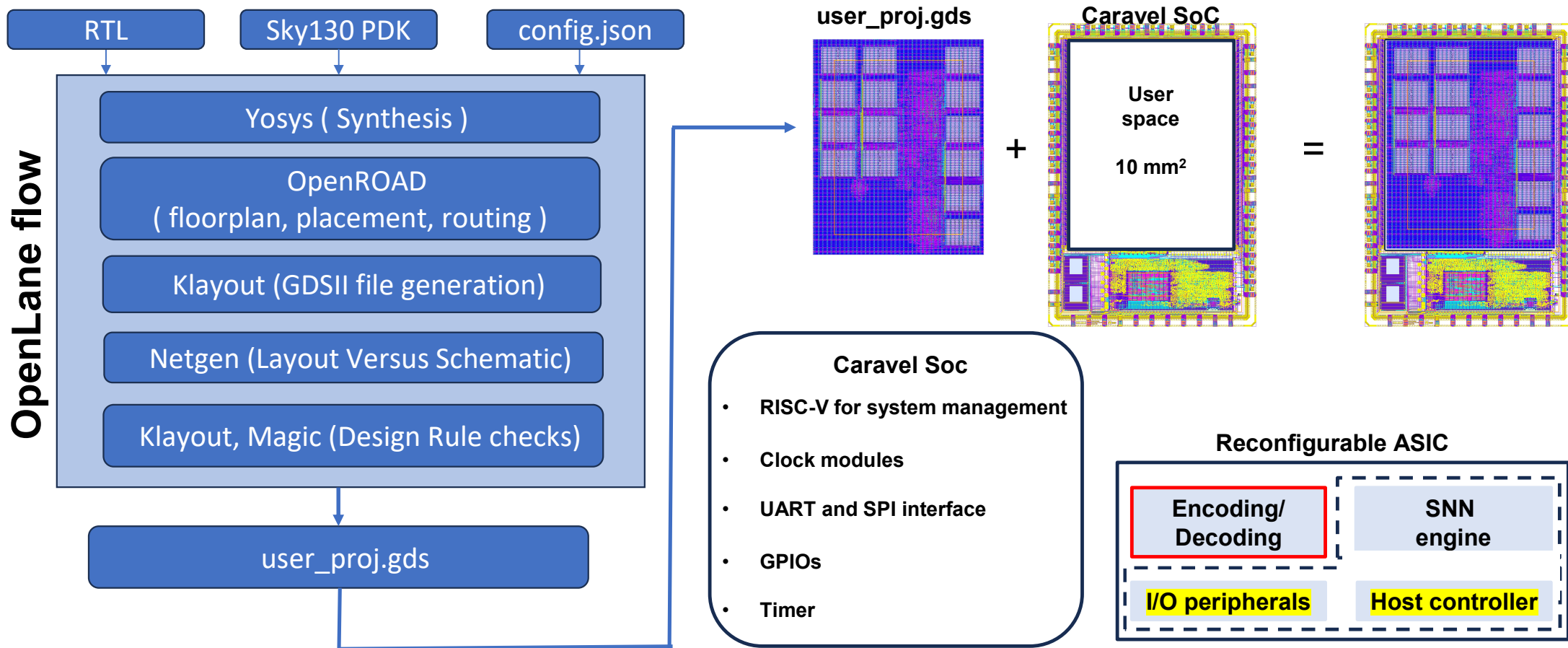
OpenROAD Flow Scripts

OpenLane

SiliconCompiler

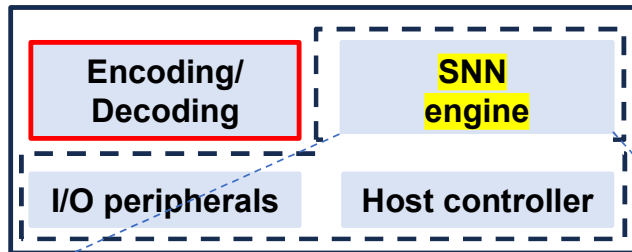


OpenLane Flow

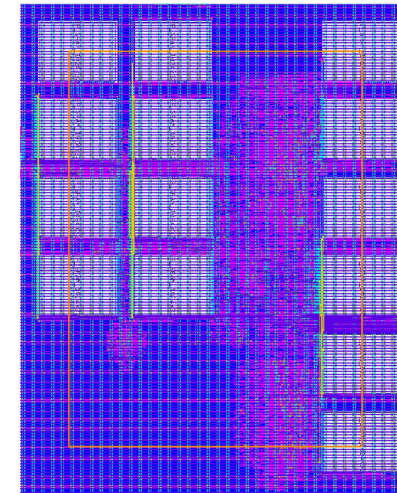
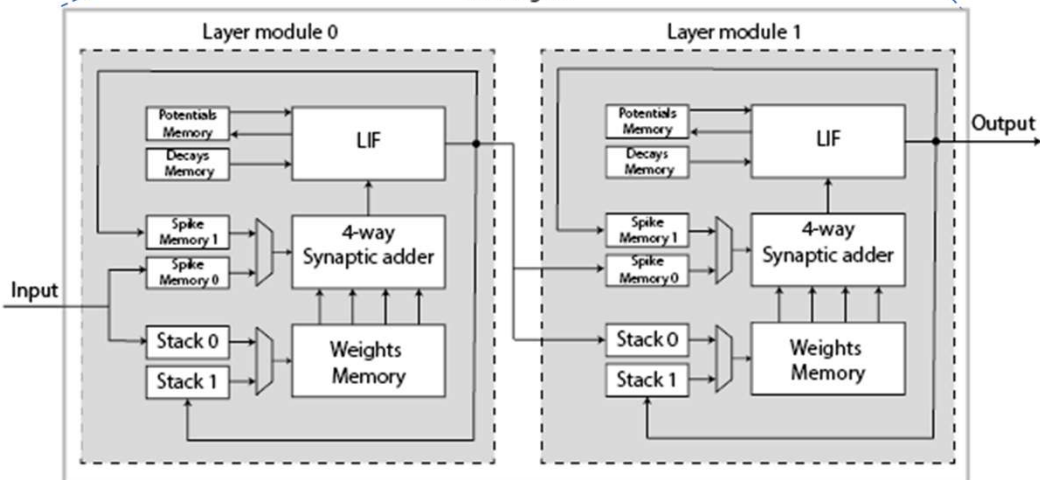


Preliminary Results

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SNN engine

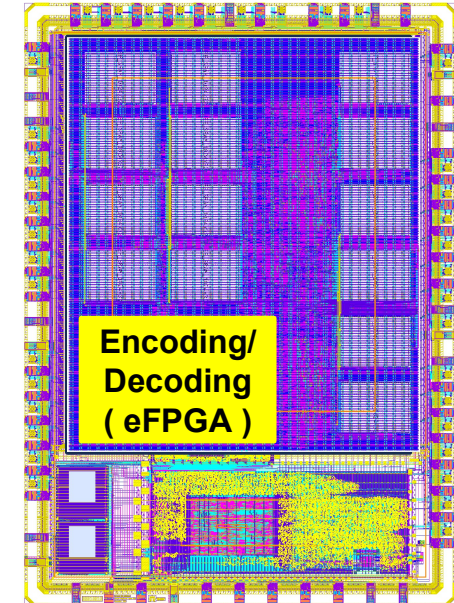
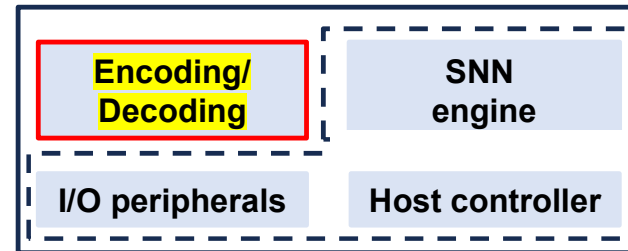


| | |
|-------------------------|---|
| Network Topology | Four dense layers (128x64x128x64x8) |
| Spiking Neurons | Leaky Integrate and Fire (LIF) |
| Area | 2550x2000 μm (46% of the available area) |
| SRAM memories | 57 KB (14 macros) |
| Total Power | 54.3 mW |
| F_{MAX} | 89 MHz |

Future Works

Future work involves completing the system by adding the encoding and decoding modules, with the intention of implementing them using eFPGA.

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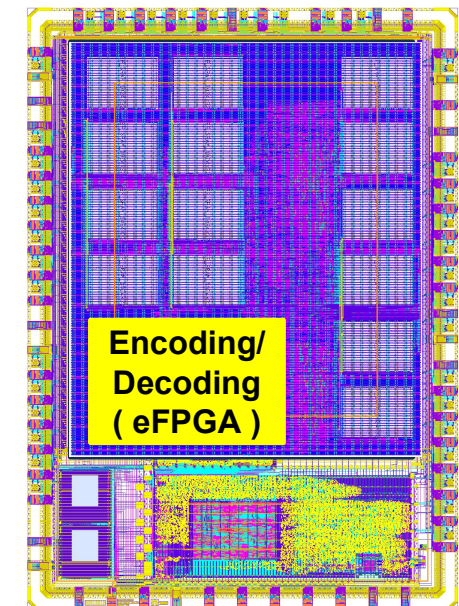
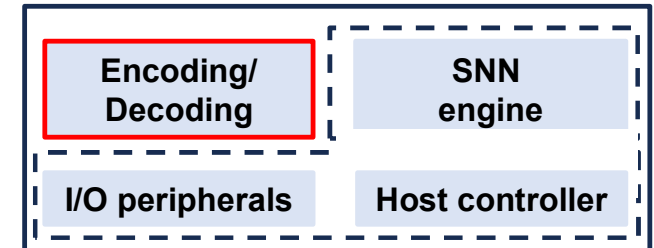
Conclusions

In this work, an accelerator for spiking neural networks integrated into a System-on-Chip (SoC) has been presented.

These initial results highlight the potential of spiking neural networks for applications on edge devices.

Although the results produced by open-source tools still have a long way to go compared to more advanced commercial tools, they have demonstrated that they can be a viable alternative to commercial solutions

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Thanks for the attention.

